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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,985	03/26/2004	Chung-Chieh Fang	24061.106 (TSMC2003.0551)	9614
43717 7590 07/23/2008 HAYNES AND BOONE, LLP 901 Main Street Suite 3100 Dallas, TX 75202				
EXAMINER BAIRD, EDWARD J				
ART UNIT 3693		PAPER NUMBER		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/809,985

Applicant(s)

FANG, CHUNG-CHIEH

Examiner

EDWARD BAIRD

Art Unit

3693

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on 10 April 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) 2,4,5,14,17,18 and 24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,6-13,15,16,19-23 and 25 is/are rejected.
- 7) ☒ Claim(s) 3 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Status of Claims

Applicant has amended claims 1, 3, 10-12, 15, 16, 19 – 21 and 25. Claims 2, 4, 5, 14, 17, 18 and 24 have been canceled; no new claims have been added. Thus, claims 1, 3, 6 – 13, 15, 16, 19 – 23 and 25 are pending in this application.

Response to Arguments

1. Applicant's arguments and amendments filed on 10 April 2008 with respect to
 - objection to drawings
 - rejection of claim 25 under 35 USC § 112, 2nd paragraph,
 - rejection to claim 2 under 35 USC § 101,
 - rejections to claims 1, 2, 4, 6, 9 – 12, 15 – 21, 24, and 25 under USC § 102(b), and
 - rejections of claims 3, 5, 7, 8, 13, 14, 22, and 23 under 35 USC § 103(a)have been fully considered.
2. Examiner agrees with amendments to drawings and accordingly, withdraws objections.
3. Examiner agrees with amendment to claim 25 in order to overcome rejection under 35 USC § 112, 2nd paragraph, and accordingly, withdraws rejection.
4. Examiner acknowledges cancellation of claim 2 and accordingly withdraws rejection under 35 USC § 101.
5. Applicant's arguments filed on 10 April 2008 with respect to rejections of claims 1, 2, 4, 6, 9 – 12, 15 – 21, 24, and 25 under USC § 102(b), **Nafeh**, been fully considered. Examiner concurs with Applicant's arguments against claim rejections under 102(b) as being anticipated

by **Nafeh**, and in turn withdraws rejection. However, additional prior art was used for new grounds of rejection against amended claims.

6. Regarding claim 1, Applicant argues that Examiner's interpretation of "*Market Authority*" of **Nafeh** as Applicant's **virtual fab** is incorrect (page 9 of 12 of Amendment). Examiner concurs with Applicants arguments but this point is also addressed by additional prior art used for new grounds of rejection.

7. Applicant argues that Examiner's interpretation of **Nafeh's** "advance purchase orders" as Applicant's **capacity contracts** is incorrect (page 9 of 12 of Amendment). Examiner concurs with Applicants arguments but this point is again addressed by additional prior art used for new grounds of rejection.

8. Applicant argues that **Nafeh** does not disclose futures contracts that are directed to "semiconductor manufacturing capacity futures based on the plurality of manufacturing capacity contracts" as required by claim 1 (page 10 of 12 of Amendment). Examiner respectfully disagrees. **Nafeh** clearly discloses the "need for additional **futures** (emphasis added) markets to facilitate the vast variety of risk management needs" [0025], and in turn, provides "a risk hedging, contract trading system" [0026]. This "risk hedging, contract trading system" is elaborated for supply chain management using "advance purchase orders" for products or services including those for semiconductor chips [0342 to 0344]. Examiner interprets *products and services for semiconductor chips* as indicative of Applicant's' manufacturing and procurement of these semiconductor chips.

9. Applicant's arguments filed on 10 April 2008 with respect to rejections of claims 3, 5, 7, 8, 13, 14, 22, and 23 under 35 USC § 103(a), **Nafeh** in view of **Hagen**, have been fully considered but moot in view of new grounds of rejection.

Specification

10. Applicant cooperation is requested in correcting any error of which applicant may become aware in the specification.

Claim Objections

11. **Claim 3** is objected to because of the following informalities: the claim recites “wherein the the virtual fab . . .”. The word “the” is recited twice and should be recited only once. Appropriate correction is required.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103 (a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claims 1, 6, 9 – 12, 15, 16, 19 – 22, and 25 are rejected under 35 U.S.C. 103 (a) as being unpatentable over **Chou et al** (US Patent No. 6,240,400) in view of **Nafeh et al** (US Patent No. 2002/0069155).

14. Regarding **claim 1**: **Chou** teaches:

- a virtual semiconductor fabrication facility (virtual fab) which provides information regarding fabrication of semiconductor devices [see at least column 1 line 56 – column 2

line 36. Examiner interprets *hub arrangement for communicating with different players* as analogous to Applicant's **virtual fab**], the virtual fab comprising, at least one communications interface with a semiconductor foundry and a plurality of manufacturing capacity contracts [see at least column 3 lines 10 – 20 and 35 – 53. Examiner interprets *semiconductor manufacturers* as analogous to Applicant's **semiconductor foundry**. Examiner notes that *bulk buyers/sellers of semiconductor manufacturing capacity* infer trading of Applicant's **manufacturing capacity contracts**. Examiner interprets *interface with input and output channels* as analogous to Applicant's **communications interface**]. **Chou** does not specifically disclose:

- a semiconductor **futures** (emphasis added) exchange coupled to the virtual fab adapted to trade semiconductor manufacturing, capacity futures based on the plurality of manufacturing, capacity contracts.

However, **Nafeh** discloses method, apparatus, and design innovations as applied to futures securities and the notion of different types of *futures contracts* tailored to specific clienteles [see at least Abstract, and 0025 – 0031]. Examiner notes that in view of the shortcomings of the prior art, there exists "a continuing need for additional *futures markets* to facilitate the vast variety of risk management needs" [0025]. Thus, Examiner interprets *risk hedging, contracts trading system* [0026] as analogous to Applicant's **semiconductor futures exchange**.

Nafeh applies his invention to Type III ("Firm-Issue" and "Intra-Industry") Contracts which are custom-tailored contracts designed in consultation with industry and firm partners [0337 and 0338]. **Nafeh** discloses setting up internal firm-specific or intra-industry *futures markets* for (1) supply chain management or (2) risk-sharing management [0341]. Such

Art Unit: 3693

contracts include those for advance purchase orders on any product, including **semiconductor chips** [0344].

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time of the **Chou** invention for to include a *risk hedging, contracts trading system* as disclosed by **Nafeh** because it allows one to trade firm-specific and intra-industry contracts (i.e. advance purchase orders). This dramatically enhances the value of the advance purchase orders to both the issuers and customers because the ability to trade these contracts avoids costly returns of unsold inventory for both manufacturers and retailers [**Nafeh** 0342 to 0344].

15. Regarding **claim 6, Chou** teaches:

- at least one entity adapted for communicating between a computer system associated with the semiconductor futures exchange and a computer system associated with the virtual semiconductor fabrication facility [see at least column 1 line 57 to column 2 line 12, and column 3 lines 5 – 20. Examiner notes that the “*Players*” include *semiconductor manufacturers* and *Bulk buyers/sellers of semiconductor manufacturing capacity*, thus being indicative of Applicant’s **computer systems** associated with an “**exchange**” and a **fabrication facility**].

16. Regarding **claim 9, Chou** teaches:

- at least one entity adapted for communicating between a computer system associated **with an external service provider** and a computer system associated with the semiconductor futures exchange [see at least column 3 lines 5 – 19. Examiner interprets “*Players*” as being inclusive of Applicant’s **external service providers**].

17. Regarding **claims 10, 11, and 12, Chou** teaches:

- computer system associated with the semiconductor futures exchange is adapted to be accessed by an investor, a customer, or a trader [see at least column 3 lines 5 – 19].

18. Regarding **claim 15**: **Chou** teaches:
 - semiconductor futures exchange is adapted to interact with a plurality of traders [see at least column 3 lines 17 – 18].
19. **Claim 16** is a method parallel to the system of claim 1 and is therefore rejected for the same reasons.
20. Regarding **claims 19, 20, and 21**: **Chou** teaches:
 - the semiconductor futures exchange is adapted to interact with a customer, an investor, and a trader [see at least column 3 lines 5 – 19].
21. Regarding **claim 22**: **Chou** teaches:
 - the virtual fab includes a plurality of entities [see at least column 3 lines 12 - 16. Examiner interprets *manufacturers of products* that incorporate chips as analogous to Applicant's **plurality of entities**].
22. Regarding **claim 25**: **Chou** teaches:
 - the semiconductor capacity futures exchange includes a trade processor for executing trades of the semiconductor manufacturing capacity futures through a market established by the semiconductor futures exchange [see at least column 3 line 65 to column 4 line 16. Examiner interprets *the deal making executor* as analogous to Applicant's **trade processor for executing trades**].
23. Claims 3, 7, 8, 13, and 23 are rejected under 35 USC § 103(a) as being unpatentable over **Chou** in view of **Nafeh** in further view of **Hagen et al** (US. Patent No. 6,748,287).
24. Regarding **claim 3**, neither **Chou** nor **Nafeh** explicitly disclose:

- the virtual fab further comprises a work in progress (WIP) reporting system for the virtual semiconductor fabrication facility.

However, **Hagen** discloses a work-in-progress (WIP) tracking system is used to coordinate a semiconductor supply chain [Abstract]. The WIP tracking receives WIP updates from semiconductor supply chain vendors and generates advanced notices based on an analysis of the WIP updates and predetermined rules [Abstract].

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time of the invention for **Chou** to include *WIP tracking* as disclosed by **Hagen** so that a user may be able to predict the value of semiconductor futures based on the availability of manufacturing time at different facilities.

25. Regarding **claim 7**, neither **Chou** nor **Nafeh** explicitly disclose:

- a manufacturing executing system used to facilitate production in the virtual semiconductor fabrication facility.

However, **Hagen** claims a method **implemented by computer** for coordinating the manufacture of a semiconductor product by a semiconductor supply chain [Hagen, claim 2]. Examiner notes that Applicant describes his manufacturing execution system (MES) as being an "**integrated computer system** representing the methods and tools used to accomplish production" [Applicant's specification 0025].

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time of the invention for **Chou** to include a method *implemented by computer for coordinating the manufacture of semiconductor products* as taught by **Hagen** so that semiconductor companies benefit by efficiently managing their supply chain [Hagen, column 1, lines 57-60].

26. Regarding **claim 8**, neither **Chou** nor **Nafeh** explicitly disclose:

- an entity associated with a specific process within the virtual semiconductor fabrication facility”.

However, **Hagen** discloses the semiconductor supply chain as possibly including many separate entities, all of which shall be referred to as **vendors** [column 1, lines 37 – 41]. Examiner interprets *vendors* as Applicant’s **entity** wherein the supply chain is analogous to Applicant’s **specific process**.

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time of the invention for **Chou** to include *vendors in a semiconductor supply chain* as taught by **Hagen** so that semiconductor companies are able to anticipate material and time requirements needed in the fabrication of semiconductor materials.

27. Regarding **claim 13**, neither **Chou** nor **Nafeh** explicitly disclose:

- the virtual semiconductor fabrication facility performs a plurality of processes associated with semiconductor fabrication.

However, **Hagen** discloses that a typical semiconductor manufacturing process includes multiple phases, starting with fabricating integrated circuits on raw silicon wafers at a wafer foundry [column 1, lines 26 – 30]. Examiner interprets *fabricating integrated circuits* as inclusive of Applicant’s **plurality of processes** associated with **semiconductor fabrication**.

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time of the invention for **Chou** to include *fabricating integrated circuits on raw silicon wafers* as taught by **Hagen** so that semiconductor companies are able to anticipate material and time requirements needed in the fabrication of semiconductor materials.

28. Regarding **claim 23**, neither **Chou** nor **Nafeh** explicitly disclose:

- the semiconductor futures exchange interfaces via the virtual fab with entities internal to and external to the virtual fab.

However, **Hagen** discloses the semiconductor supply chain as possibly including many **separate entities**, all of which shall be referred to as vendors [column 1, lines 37 – 41]. Examiner interprets *separate entities* as inclusive of Applicant's **entities internal to and external to the virtual fab**.

Therefore, it would have been obvious to a person having an ordinary skill in the art at the time of the invention for **Chou** to include *separate entities in a semiconductor supply chain* as taught by **Hagen** so that semiconductor companies are able to anticipate material and time requirements needed in the fabrication of semiconductor materials.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ed Baird whose telephone number is (571) 270-3330. The examiner can normally be reached on Monday - Thursday 7:30 am - 5:00 pm Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Kramer can be reached on (571) 272-6783. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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